



FORM PTO-1449 (SUBSTITUTE)	Attorney Docket No.: GR 99 P 5374	RCE of Applic. No. 09/729,069
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Applicant Nicolas Nagel et al.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	RCE Filing Date March 4, 2003	Group Art Unit 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
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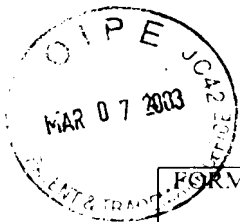
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

DV	O	Aoyama et al.: "Interfacial Layers between Si and Ru Films Deposited by Sputtering in Ar/O ₂ Mixture Ambient", Jpn. J. Applied Physics, Volume 37, 1998, pp. L242-44.
DV	P	Onishi et al.: "High Temperature Barrier Electrode Technology for High Density Ferroelectric Memories with Stacked Capacitor Structure", J. Electrochemical Society, Volume 145, No. 7, July 1998, pp. 2563-64.
EXAMINER	DATE CONSIDERED	
<i>ghulard</i>	05/01/03	

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DV	O	Onishi et al.: "A New High Temperature Electrode-Barrier Technology on High Density Ferroelectric Capacitor Structure", IEDM 96, pp. 699-702.
DV	P	Kudo et al.: "A High Stability Electrode Technology for Stacked SrBi ₂ Ta ₂ O ₉ capacitors Applicable to Advanced Ferroelectric Memory", IEDM 96, pp. 609-12.

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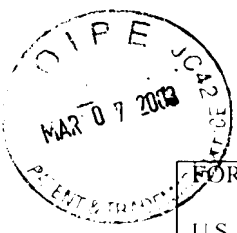
DV	O	Cho et al.: "Preparation and Characterization of Iridium Oxide Thin Films Grown by DC Reactive Sputtering", Jpn. J. Applied Physics, Volume 36, 1997, pp. 1722-27.
DV	P	Jeon et al.: "Thermal Stability of Ir/Polycrystalline-Si Structure for Bottom Electrode of Integrated Ferroelectric Capacitors", Applied Physics Letter 71 (4), July 28, 1997, pp. 467-69.

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DV	O	Bhatt et al.: "Novel High Temperature Multilayer Electrode-Barrier Structure for High-Density Ferroelectric Memories", Applied Physics Letter 71 (5), August 1997, pp. 719-21.
DV	P	Saenger et al.: "Buried, Self-Aligned Barrier Layer Structures for Perovskite-Based Memory Devices Comprising Pt or Ir Bottom Electrodes on Silicon-Contributing Substrates", J. Applied Physics, 83 (2), January 15, 1998, pp. 802-813.

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